Two-Octave Bandwidth Monolithic Analog Phase Shifter

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Abstract— **The cascaded-match reflection-type phase shifter (CMRTPS) was recently introduced to utilize the full bandwidth of its 3-dB quadrature directional couplers. A monolithic realization of the CMRTPS is presented that maintains a high level of performance over two octaves, while using experimental one octave bandwidth offset multilayer folded directional couplers. Standard GaAs foundry processing was used to fabricate the MMIC. At the 10-GHz center frequency, the measured relative phase shift varied from 0 to 98°, with a decreasing bias potential from 0 to −10 V. Here, a maximum rms phase error of ±2.8° is maintained across the 4.4 to 16.1 GHz frequency range, for all bias levels.**

I. Introduction

THE CASCADED-MATCH reflection-type phase shifter (CMRTPS) was recently introduced [1] to significantly widen the bandwidth of traditional narrow-band (<10%) high-performance analog reflection-type phase shifters (RTPS's). Here, two RTPS's are cascaded, where the nonlinear performance of each stage compliments the other. In order to obtain a low phase and amplitude error over the full octave bandwidth, at all levels from 0° to over 180°, it was found that the following conditions have to be satisfied by the reflection terminations.

1) The resonant frequency of the second stage reflection termination must correctly scale that of the first stage, at the zero bias potential.
2) The change in the resonant frequency of the second-stage reflection termination must correctly track the change in that of the first stage.
3) The reflection coefficient of the second-stage reflection termination must have a phase angle whose gradient, with respect to frequency, correctly scales that of the first stage, at their respective frequency of resonance.

The simulated results for a one octave bandwidth design [1], employing one octave bandwidth Lange couplers, and a one decade bandwidth MMIC design [2], employing one decade bandwidth active circulators, have been reported.

In this letter, a monolithic realization of the CMRTPS is presented which maintains a high level of performance over two octaves, while using experimental one octave bandwidth offset multilayer folded directional couplers [3].

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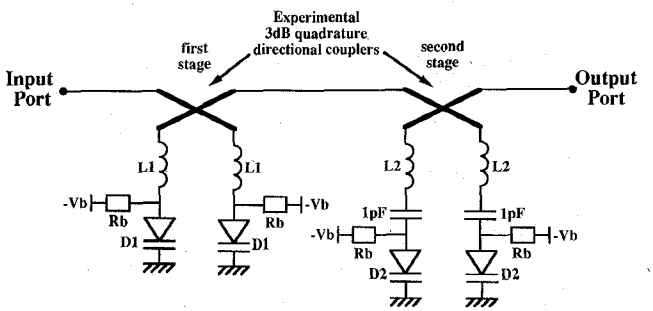

Fig. 1. Topology for the two-stage CMRTPS.

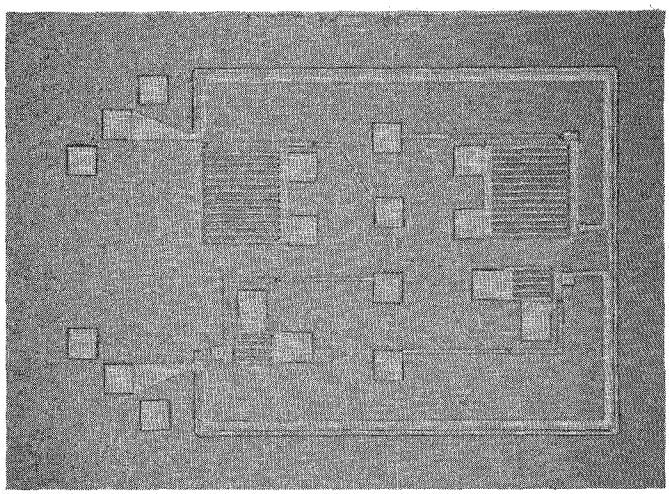

Fig. 2. Photomicrograph of the CMRTPS realization.

II. Monolithic Realization

The topology for the two-stage CMRTPS is shown in Fig. 1. The 4.4–16.1-GHz phase shifter was fabricated at the GEC-Marconi (Caswell) foundry, using their standard F20 process, which uses two metal layers and facilitates through-GaAs via holes. A photomicrograph of the GaAs MMIC, with its maximum dimensions of $3.0 \times 2.0 \times 0.2$ mm^3, is shown in Fig. 2.

Experimental one octave bandwidth offset multilayer folded 3-dB directional couplers are employed, since they have been shown to maintain an excellent phase quadrature performance when folded and require less than half the chip area — when compared to conventional Lange couplers.

The cross-section of the coupler is illustrated in Fig. 3. The conductor tracks are 30-μm wide. The lower conductor layer track is 0.5-μm thick and normally used for the underpass connections of spiral inductors and to produce Schottky

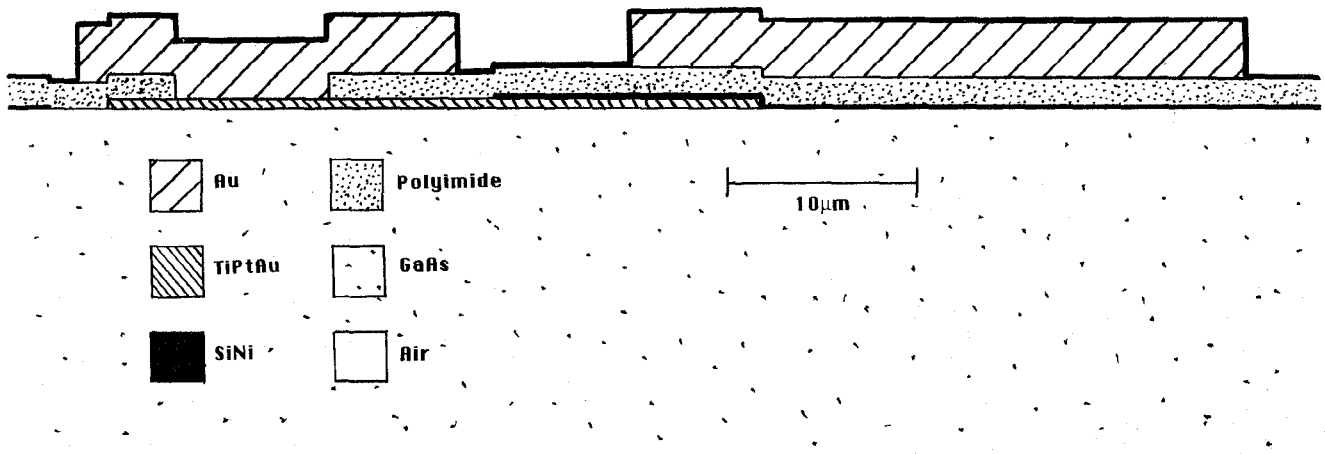

Fig. 3. Cross-section of the offset multilayer coupler.

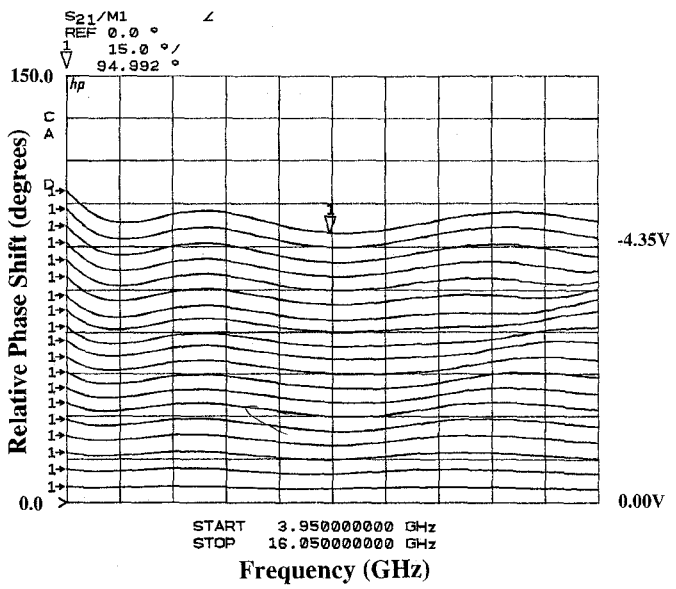

Fig. 4. Relative phase shift responses.

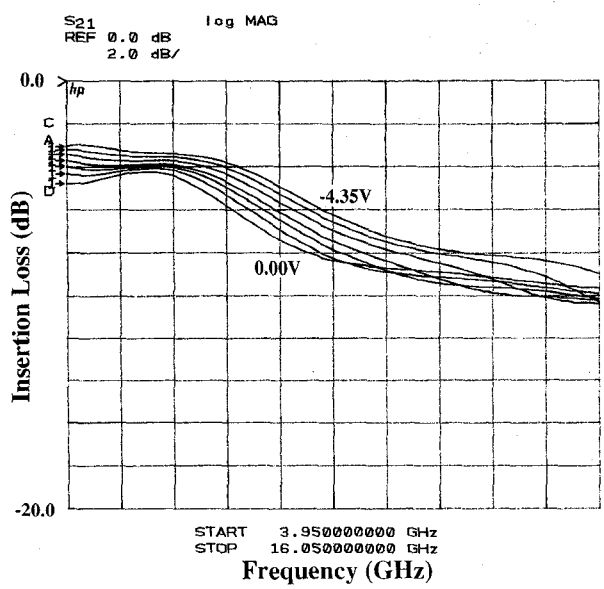

Fig. 5. Insertion loss response.

barrier junctions. The upper conductor layer track is 3-μm thick and normally used for plating-up Ohmic contacts and forming transmission lines. The tracks are separated by a thin polyimide layer, with a small dielectric constant. This layer is traditionally used for realizing low value capacitors.

The direct two-port measurements and subsequent modeling strategies for this multilayer coupler have been fully described in detail [3].

Abrupt interdigitated planar Schottky varactor diodes (IPSVD's) can be realized by connecting together the drain and source terminations of a standard library cell MESFET — resulting in a single Schottky junction. The bias potential is then applied across the drain/source (cathode) and gate (anode) terminations. High value resistors, $R_b \sim 6\text{K}\ \Omega$, were used to prevent RF leakage and as forward bias current limiters.

The IPSVD's used in the first stage, D_1, and second stage, D_2, are derived from 12×300 μm and 6×150 μm ion-implanted 0.5 μm gate-length MESFET's, respectively. Techniques for the accurate characterization of these devices have been reported [4], [5] and successfully used in the modeling of this phase shifter.

III. Measured Results

The MMIC phase shifter was measured on a Cascade Summit 9000 probe station using a Hewlett Packard 8510B automatic network analyser. Fig. 4 and Fig. 5 show the relative phase shift responses and insertion loss responses, respectively, for various bias levels. At the 10-GHz center frequency, the relative phase shift varies from 0 to 90°, with a decrease in the applied bias potential from 0 to -4.35 V, and 0 to 98°, with a decrease in the applied bias potential from 0 to -10 V. This latter level of relative phase shift is achieved with a capacitance ratio of $C(0)/C(-10\ \text{V}) = 4.5$, using the F20 process. The maximum rms phase error is only $\pm 2.8°$ across the 4.4–16.1-GHz frequency range, at all bias levels.

The measured input return loss is better than 9 dB across the 4.8–16.1-GHz frequency range, at all bias levels. This modest input match performance can be directly attributed to the

poor experimental design used in the coplanar waveguide-to-microstrip transitions. A very flat group delay response of 100 ps ±4 ps was measured in the 8.8–16.1 GHz frequency range. This characteristic is useful for pulsed radar applications.

IV. Conclusion

A monolithic realization of a two octave bandwidth CM-RTPS has been demonstrated, employing experimental one octave bandwidth offset multilayer folded 3-dB directional couplers to replace the conventional Lange couplers. Standard GaAs foundry processing was used to fabricate the MMIC. An excellent rms phase error performance of ±2.8° was measured across the 4.4–16.1 GHz frequency range, for all levels of relative phase shift up to 98°.

In the second prototype, hyperabrupt IPSVD's [6] will be employed to double the maximum relative phase-shift level. In addition, more bends will be introduced into the multilayer directional couplers to significantly increase the level of integration.

Acknowledgment

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